Layout Implementation guide for SMA Test Stations

D McMillan

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Power Supplies

Test equipment should have a higher tolerance on power supplies than the final application to allow for the most accurate test conditions.

Largest allowable tolerances:

- Final application: VM ±100mV
- Test stations: VM ±50mV

Power supply cables and tracks to be low resistance.

Test boards have more space for extra bulk capacitance for higher noise immunity for test electronics in production environments.

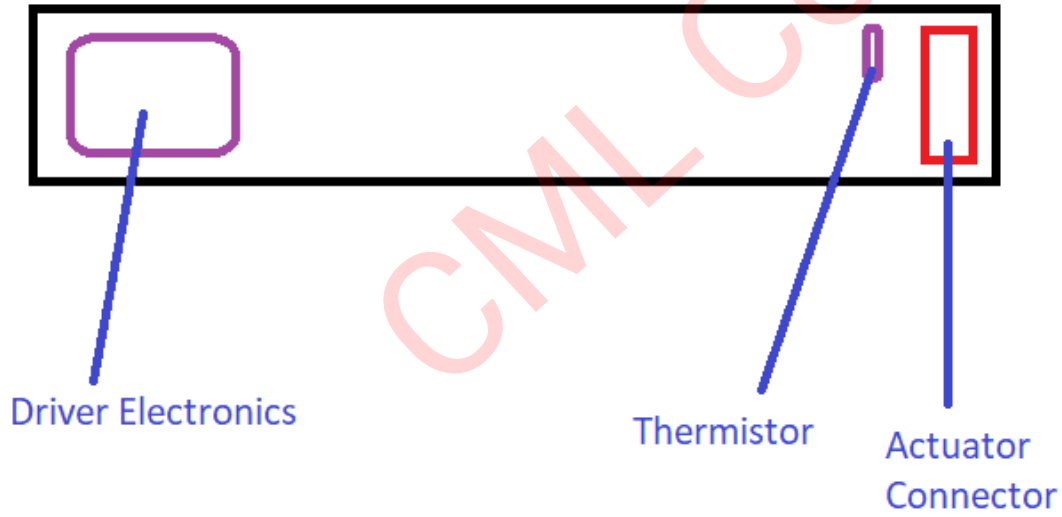
Thermistor

- The thermistor must be placed close to the screening can, or inside the actuator. Ideally close to the actuator pins.
- If there is no actuator then placing the thermistor close to actuator connector pins is the next best option.
- The thermistor cannot be placed close to any electronics that might increase its temperature such as the driver IC. The minimum distance between thermistor and drive IC should be 5mm
- Do not cover the thermistor with any material

Thermistor Example

Long boards or flexi boards should minimize the required length to keep SMA track resistances down.

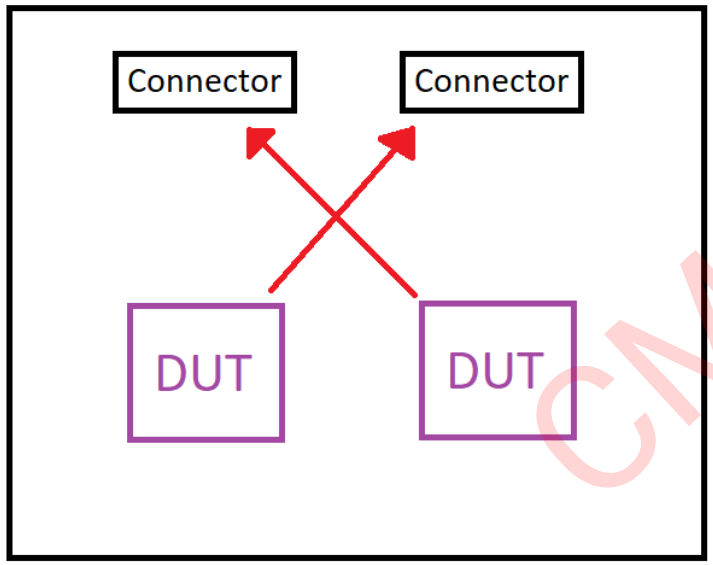
Thermistor should be placed close to the actuator connector



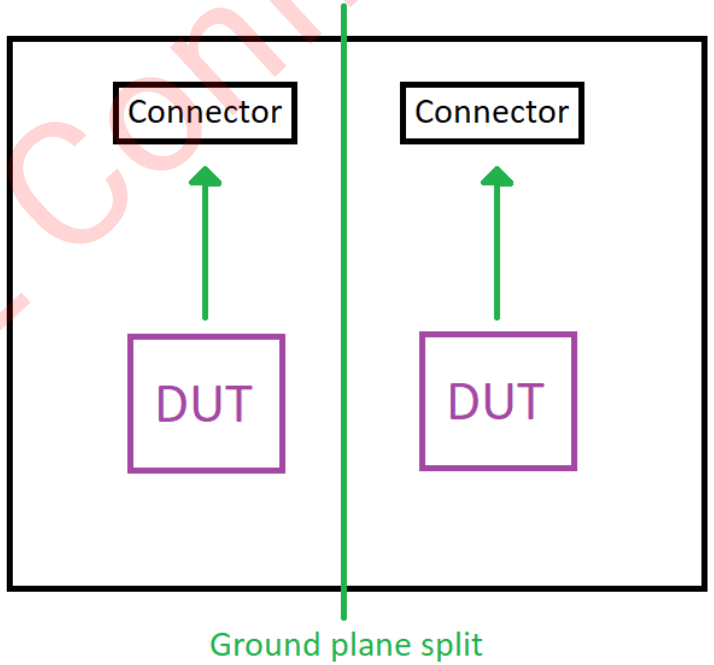
Multiple Device - Test Separation

- Split ground planes between the 2 different devices
- Do not cross over connections between DUT and connectors
- No signals to go over the ground plane split

Bad Example:



Good Example:



PCB and Cable Recommendations

- The PCB must be robust to electromagnetic emissions
- Upper and lower layers of the PCB must be flooded as much as is possible with DGND
- There should be no current loops in the power delivery path
- Multiple connections should be done with cables rather than individual loose wires.
- Cable should be at least 0.4mm diameter (26AWG) for power or SMA connections

SMA Track Recommendations - 1

- Care needs to be taken to ensure the PWM power switching traces are kept away from sensitive analogue traces to avoid unwanted interference

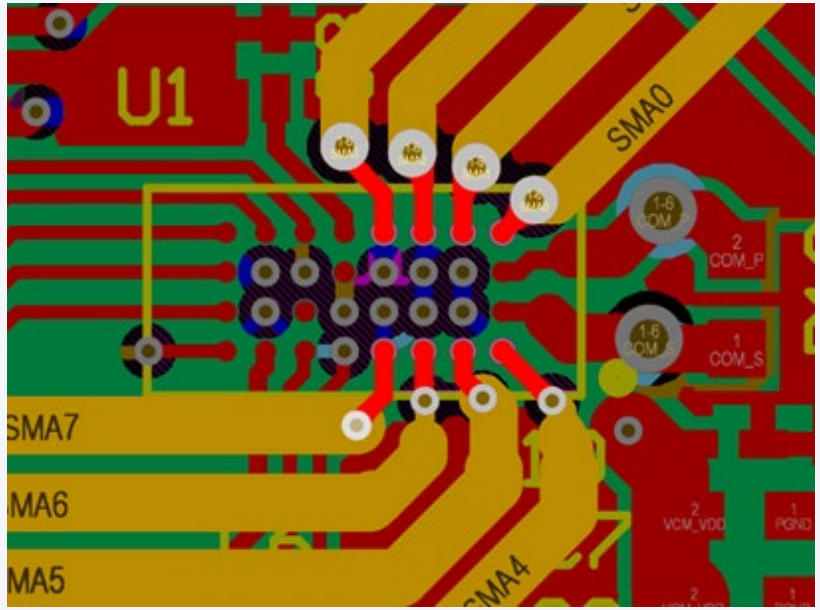
- Avoid routing the SMA power traces close to any sensitive analogue power traces or MIPI traces

- Any electromagnetic emissions from the SMA drive traces must be minimised, by eliminating current loops in the power delivery path

SMA Track Recommendations – 2

Layout priorities for SMA tracking:

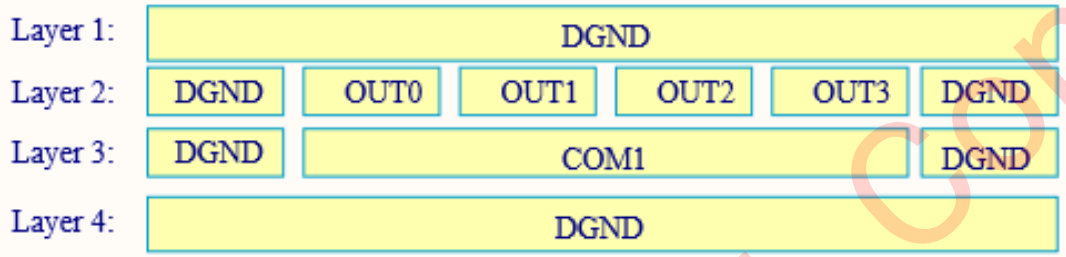
- Traces OUT0~OUTn and COM must be kept as short as possible with wide tracks to keep track resistances low as possible
- Minimal inductance around VM → COM → actuator → OUTx → PGND loop to aid quick settling time for resistance measurement
- It is recommended that OUTn and COM traces are routed on internal layers
- Minimal inductance between the actuator and decoupling capacitors, to reduce high frequency conducted noise
- Reducing the loop size by putting tracks on adjacent layers will help to minimise inductance

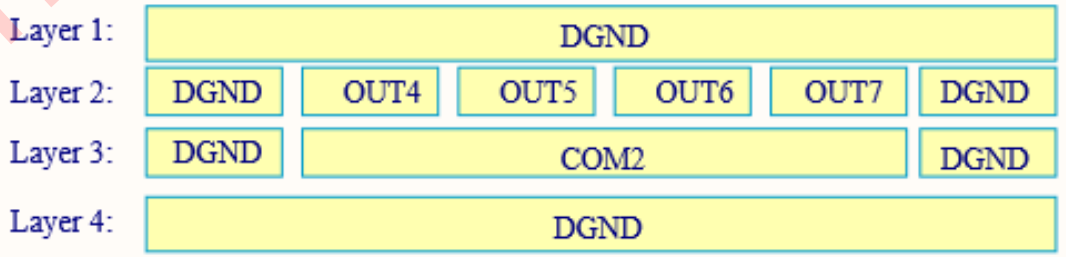


SMA Track Recommendations – 3

- DGND does not need to be between SMA tracks.

- Ideal SMA tracking example: -



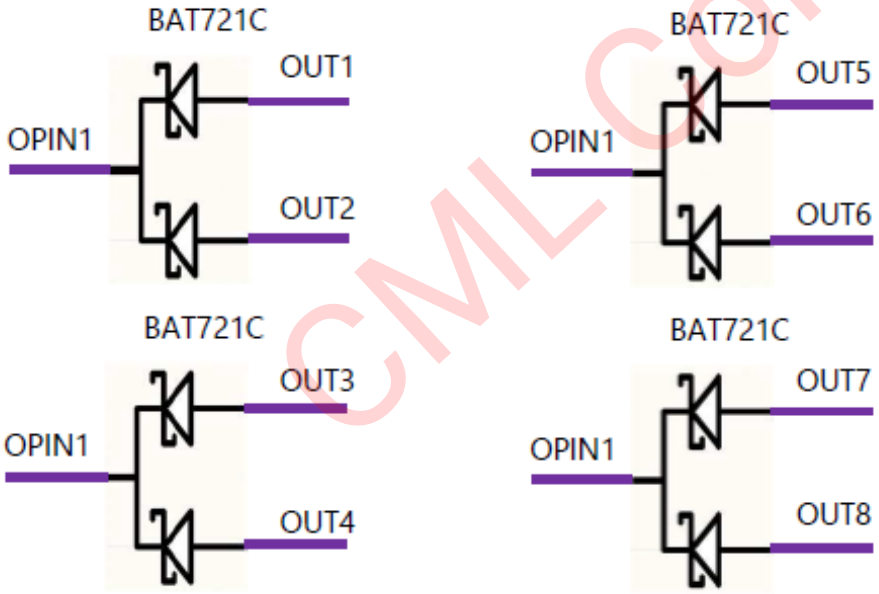


Some applications require that COM1 and COM2 are connected to each other which should be done close to the driver IC.

Snubber Diodes for SMA

- Test systems with long cables that contain SMA tracks require the addition of snubber diodes. The cable inductance can be high, causing voltage spikes at the driver IC outputs when switching currents. This occurs in all driver ICs and without snubber diodes the driver IC can be damaged.

- The snubber diodes must be placed close to the driver IC



Gyro layout advice

- Tracks from the gyro should be straight out for 0.8mm before turning or joining a plane

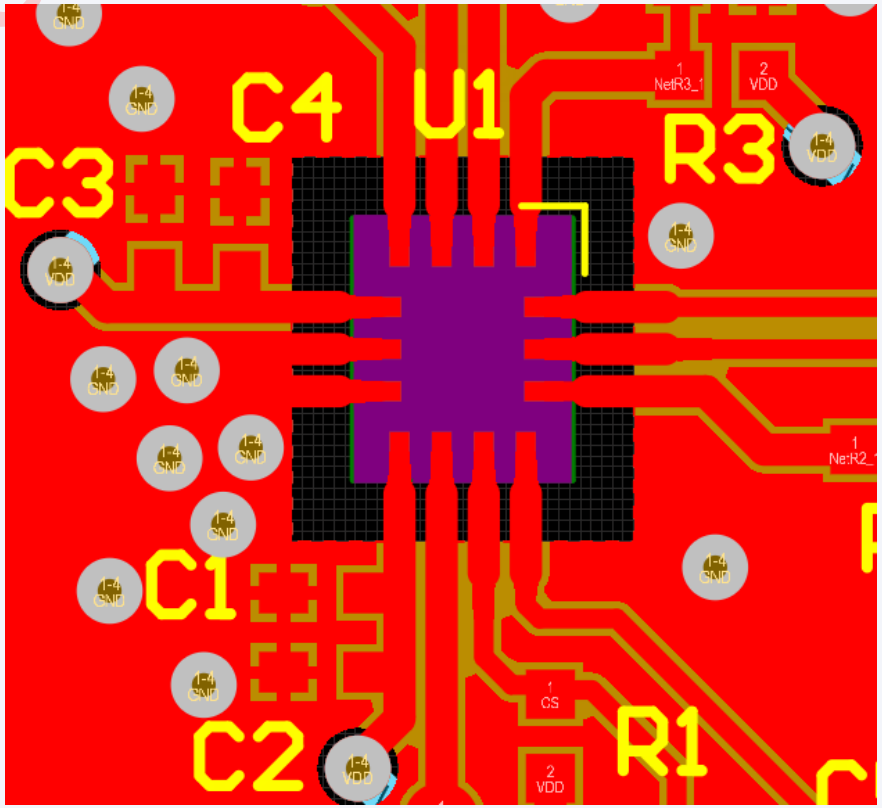
- Tracks out from gyro should all be equal width

  (Some gyros require thick tracks and good ground connections as well)

- No copper or solder resist below the gyro or within the 0.8mm exclusion area around the gyro

- No vias placed below the gyro or within the 0.8mm exclusion area around the gyro

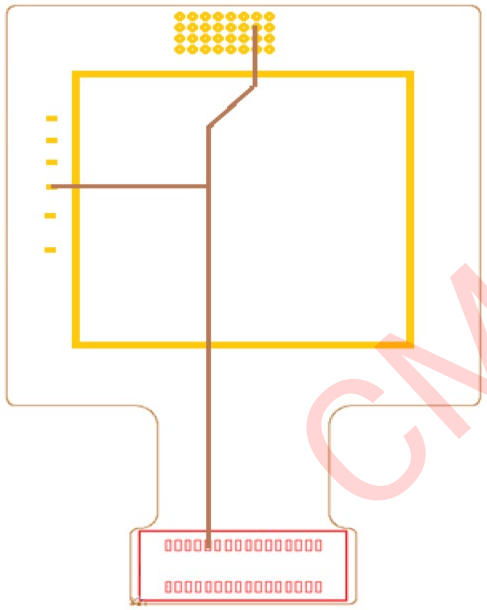
Please contact the gyro manufacturer for the latest information on layout guidelines!



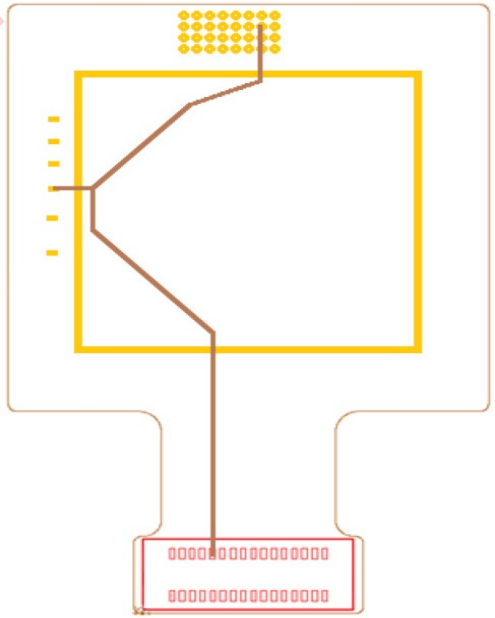
MCLK Routing

- MCLK should be routed as one continual track
- Forks should be avoided as this creates a risk of clock reflections

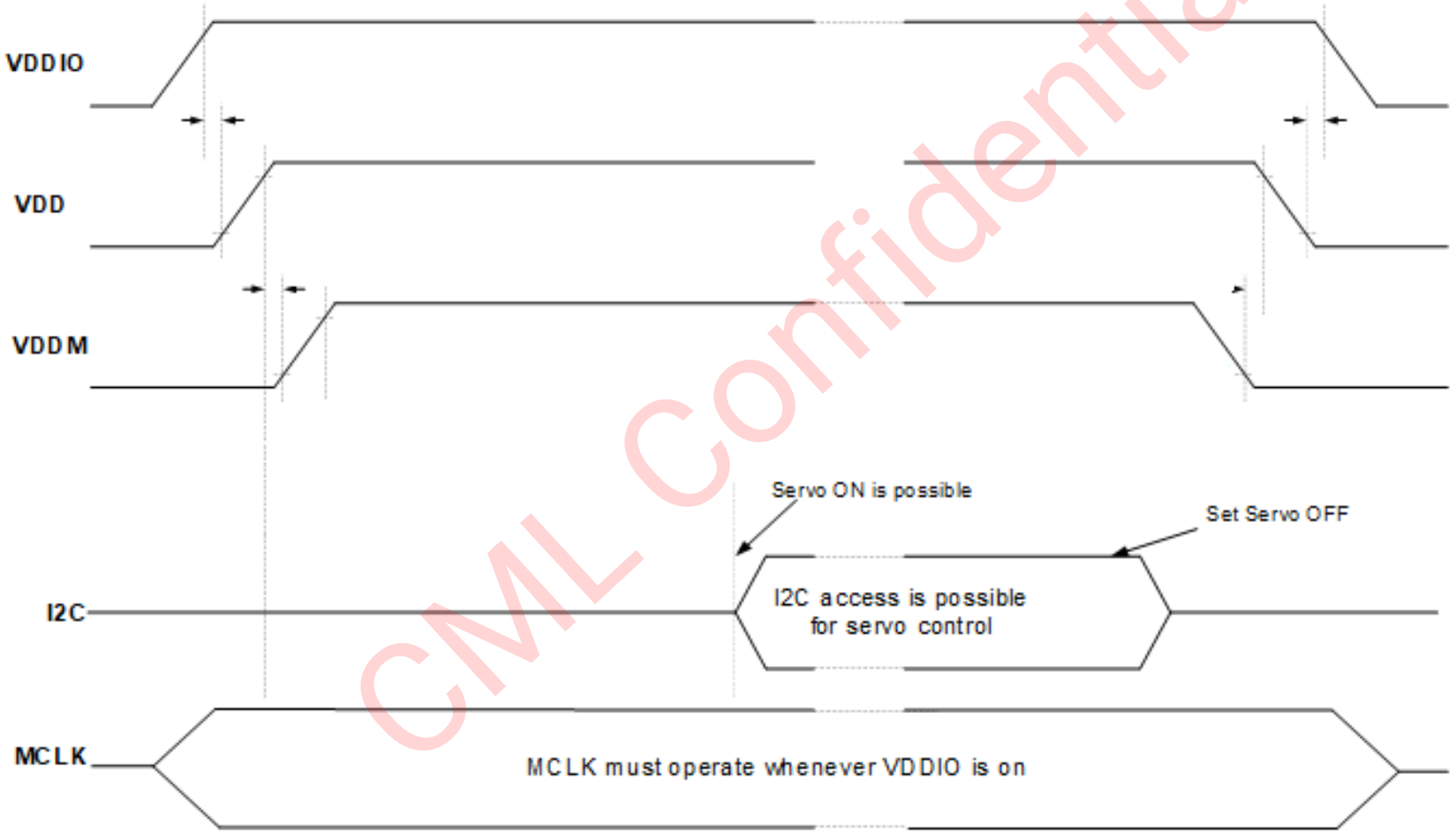
Fork – NG



No Fork – OK



Typical Power On/Off sequence



Document revision history

Revision	Date	Author	Comments
1.0	15/03/2024	D McMillan	Initial release